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Investigation of digital to analog converter to improve Integrated Circuits

Abstract

The purpose of this study is to investigate a digital-to-analog converter to improve integrated circuits. This calibration eliminates redundant comparators and thus reduces the area. Reference voltage generators, which run on resistive ladders in conventional ADCs, are eliminated thanks to the use of CDAC with interpolation in comparators. The measured DNL and INL (with and without calibration) are shown in Figure 13. Prior to calibration, the DNL and INL each reach 3 LSBs. After calibration, they are reduced to 0.8 LSB. The measured range after calibration is shown in the figure. Here, the sampling frequency is 1 GS/s, and the input signal frequency is 501 MHz. The SNDR is 32.8 dB, resulting in 5.16 ENOB at Nyquist frequency.

Keywords: *Subranging, Analog to digital conversion, Integrated Circuits, foreground calibration.*

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Introduction

High-speed analog-to-digital converters (ADCs) with a resolution of about 6 bits have been used for oscilloscopes and read channels of data storage devices (such as HDDs and DVD drives) since the 1990s [1], [2]. Currently, such ADCs are used in Ethernet, power cord connections, and optical communication systems [3]. Flash ADCs are traditionally used for these applications due to their high speed. However, flash ADCs have one drawback: their area and power consumption increase exponentially with resolution [4]. In addition, as the number of comparators increases, the ADC input capacity increases, which often limits performance [5]. Sub-architectures have large and small decisions in which the outcome of the large decision determines the scope of the small decision conversion. This architecture potentially gives you speed, area, and power, which is about half the distance between flash ADC and SAR ADC. Thus, the subset architecture can minimize the problems caused by a wide range of time-consuming SAR ADCs [6]. In addition, using different samplers for large and delicate decisions [4] causes sampling errors between decisions. Since sampling errors cannot be compensated by calibrating comparators, redundant comparators are needed [7].

To solve these problems, this paper proposes a scheme in which reference voltages are generated for large and good decisions without using rugged ladders. The proposed scheme eliminates sampling error by using the same CDACs to capture the input signal for both decisions. In addition, a calibration method is used to reduce the error due to the compensating voltages of the comparators.

Another problem arises because a ladder generates resistor reference voltages [8]. Because the ladder nodes are instead of intermediate potentials or the resistance of the switches is high, this increases the settling time after the reference voltage changes. Although increasing the switch transistor size can reduce the switch's resistance, additional parasitic capacities and the effects of higher injection and charge per hour limit ADC performance [9]. The resistance of the reference ladder cannot be reduced too much as the static current of the ladder increases. Alternatively, large chip capacities connect the ladder nodes to the ladder output impedance or reduce the impedance level.

To solve the problems in the switches connected to the potential intermediate nodes, CDACs have been used together with an interpolation method for good decisions [10]. In this scheme, the switches used to generate the reference voltage in the CDAC are connected to both or not to the middle voltage of the resistance ladder. In addition, using an interpolation method, only two CDACs are needed to guide all comparators when making a good decision. Although settling time issues have been eliminated due to the presence of resistance ladders in good decision-making [10], different samplers are used for large and good decisions. So sampling errors occur between decisions, and redundancy is still necessary.

The comparator array comprises seven dynamic comparators that share their inputs and generate a seven-bit thermometer code. Each comparator uses two input-differential pairs to form a weighted sum of the input signals before comparison. As described in the next section, the threshold level of the comparator is determined by the total weight, which is measured by the input devices.

CIRCUIT IMPLEMENTATION

In the proposed sub ranging ADC (Fig. 1), the input signal is sampled into the capacitors of CDACs once, and the same sampled charge is used for the coarse and fine decisions. Interpolating the CDACs' outputs in the comparators generates threshold levels for both decisions, eliminating the resistive ladder. Also, the same comparator array performs the coarse and fine decisions by using a calibration setting dedicated to each decision, reducing the area occupied by the comparators.

The switch control circuits control the switches in the CDACs by using the state signals S, HC, and HF. The control circuits also refer to the output of the comparator array T1 to T7 obtained in the coarse decision to generate appropriate

threshold levels for the fine decision. Signals S, HC, and HF are generated by a clock-generator circuit (CLK Gen.) based on a 2-GHz input clock signal, CLK. Signal S has a frequency of 1 GHz with a duty ratio of 25%, HC has 1 GHz and 25%, and HF has 1 GHz and 50% (Fig. 2).

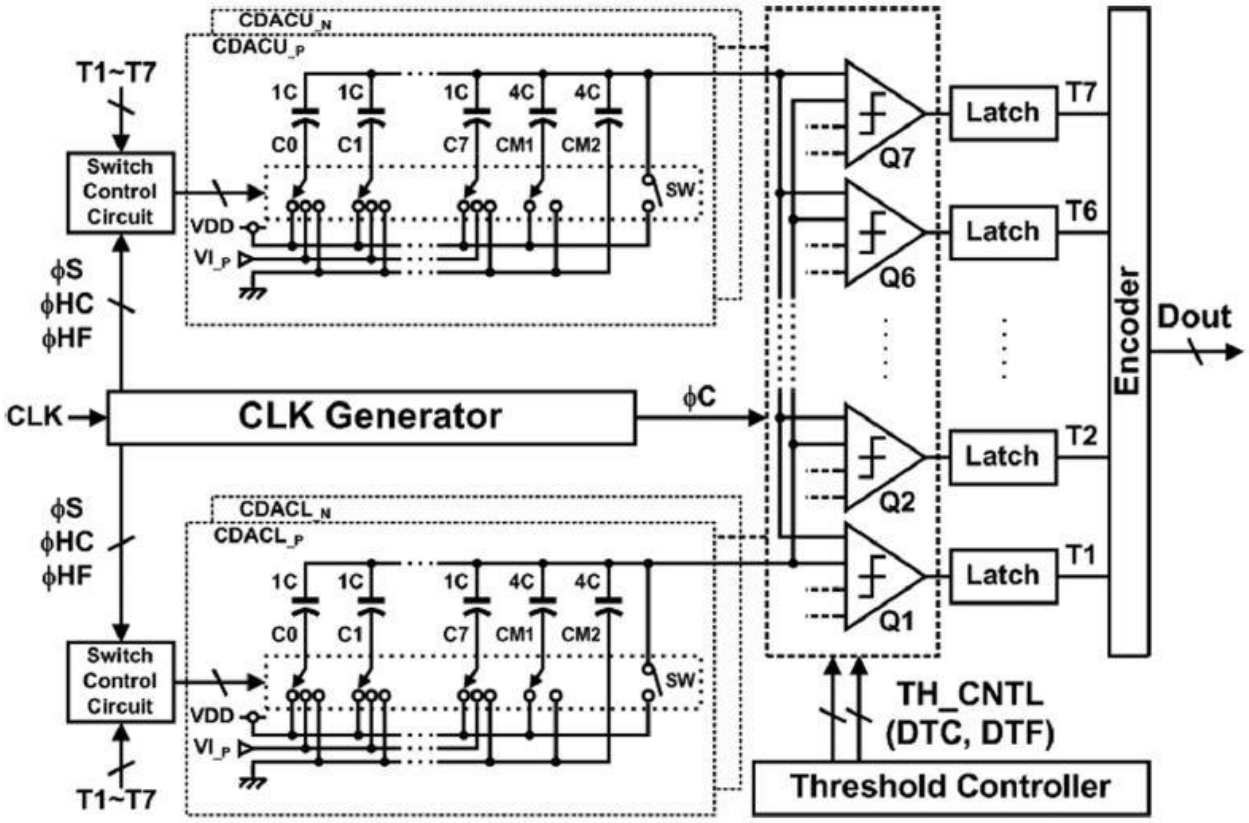

Fig. 1. Block diagram of the proposed ADC.

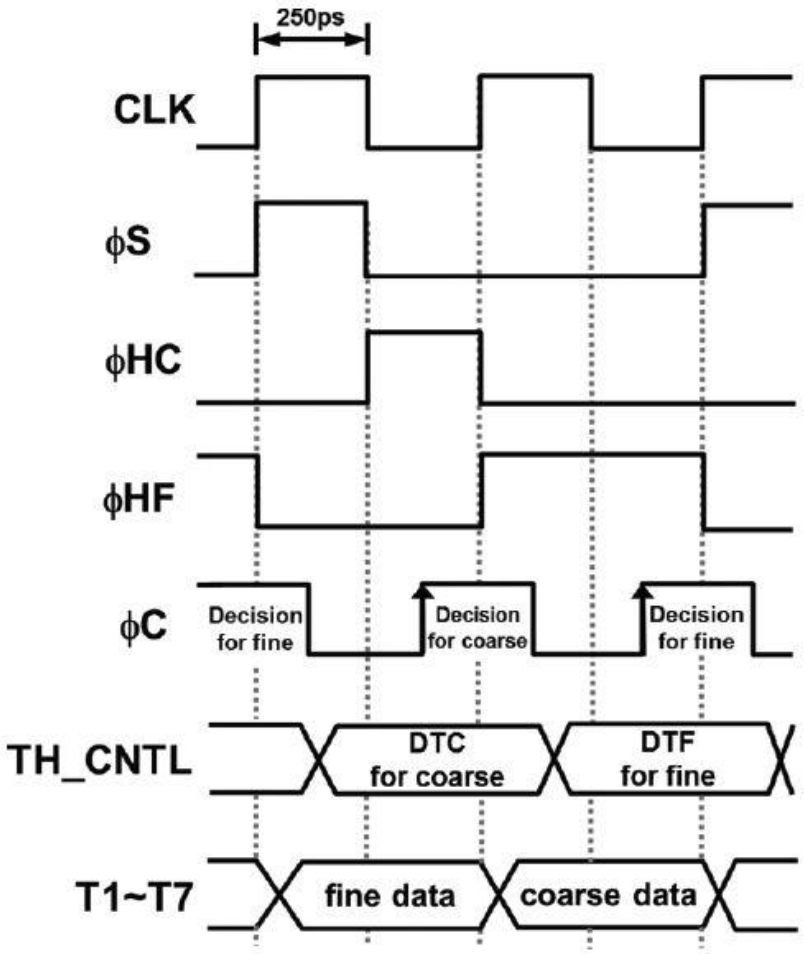

Fig. 2. Timing diagram of the proposed ADC.

To generate an appropriate reference level in the comparator, two differential CDACs, i.e., CDACU and CDACL, composed of two single-ended CDACs (Fig. 3), are used. CDACU is composed of $CDACU_P$ and $CDACU_N$, and CDACL is composed of $CDACL_P$ and $CDACL_N$. Although the analog signal path is fully differential, as shown in Figs. 3 and 4, single-ended representations referring to positive half circuits are often used for simplicity. When needed, a suffix $_P$ or $_N$ is used to specify whether a positive or negative half-circuit is being referred to.

To generate the voltage for the coarse decision, the bottom plate of CM1 is connected to GND, and the bottom plates of C0 to C7 of CDACU are connected to VDD. The bottom plates of C0 to C7 of CDACL are then connected to GND. If the parasitic capacitance at the CDAC output node is neglected, the CDAC output voltages (VU_C and VL_C) can be expressed as:

$$VU_C = VCM - \tfrac{1}{2} * (VI - VDD) \quad (1)$$

$$VL_C = VCM - \tfrac{1}{2} * VI \quad (2)$$

$$VCM = \tfrac{3}{4} * VDD \quad (3)$$

The dependence of the coarse-decision CDAC outputs on the input voltage (VI) is conceptually illustrated in Fig. 4(a).

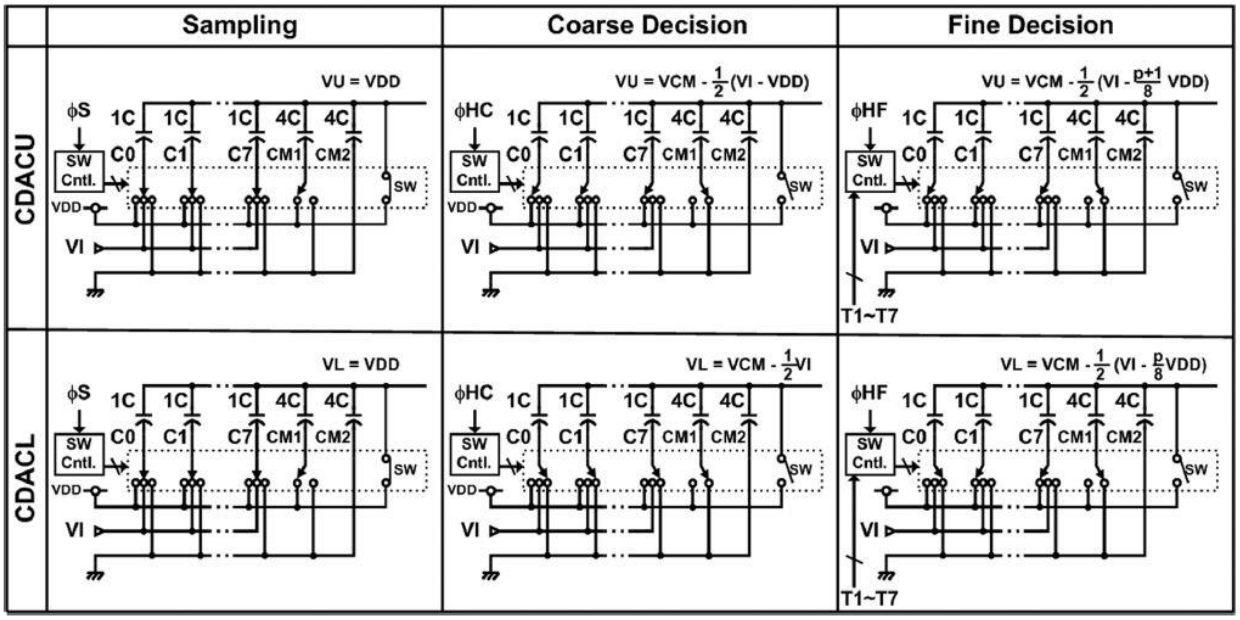

Fig. 3. Operational diagram of CDACs.

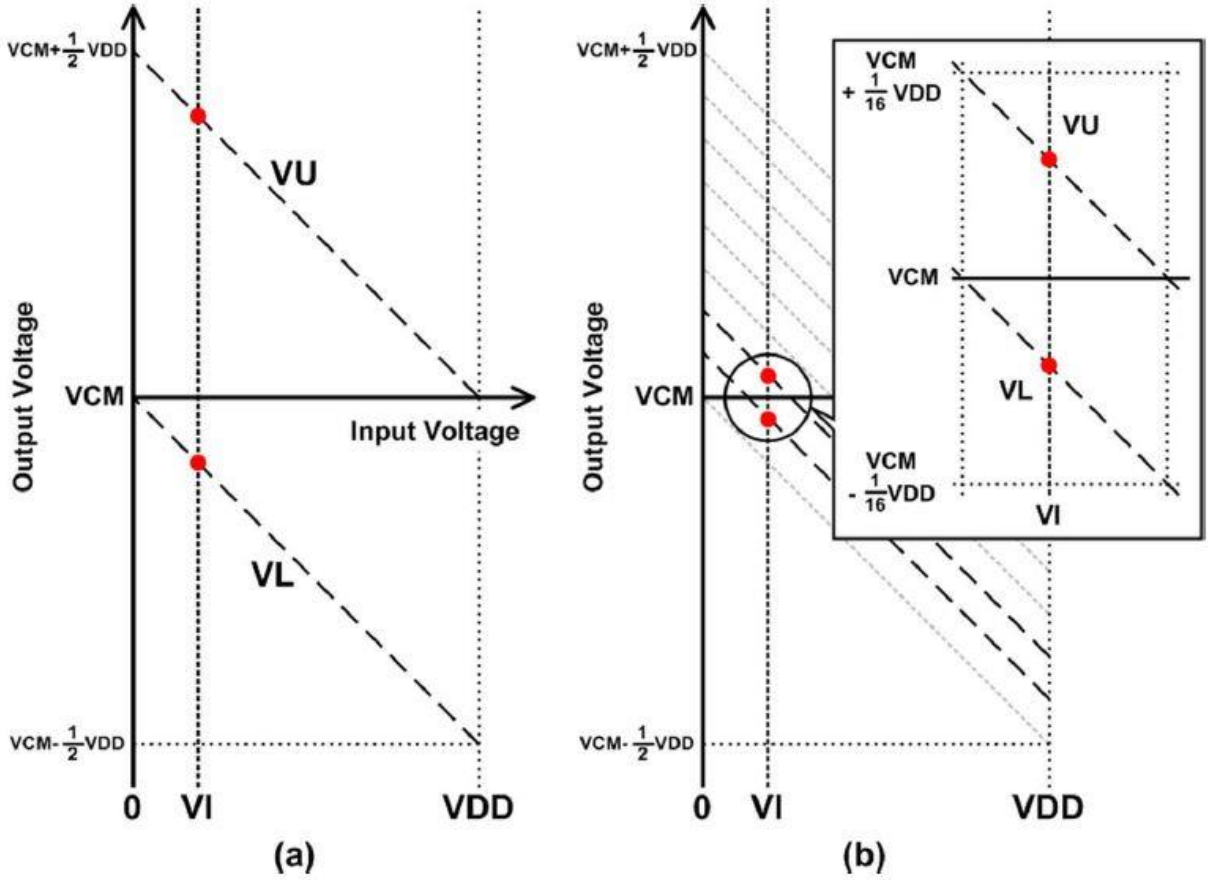

Fig. 4. Conceptual diagram of CDAC output (a) for coarse decision and (b) for fine decision.

Fig. 4(b) is a conceptual diagram of the outputs VU and the CDAC versus input voltage VL for the fine decision. In our design, the CDACs do not generate an excessively high gate voltage that would cause reliability issues because there is parasitic capacitance at their output nodes.

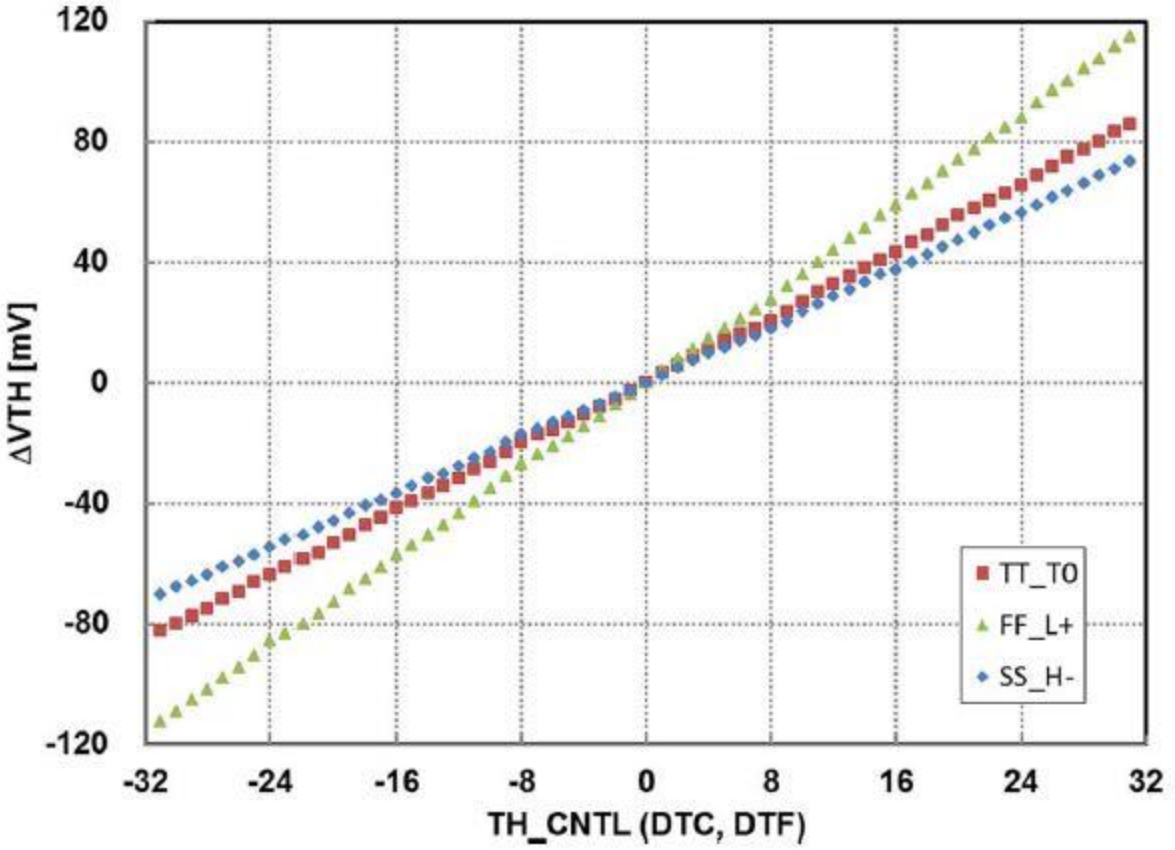

Fig. 5. Simulated controllable range of the comparator's threshold level vs. control code.

To calibrate for a good decision, the CDACs are set so that all the input voltages of the comparators are converted to a common state voltage VCM and the threshold controller follows the control code DTok that forces the comparator to generate H and L with probability. Equals (Figure 6) are produced by connecting the bottom plates C0 to C7 to CDACU and C0 to C7 to CDACL during the sampling period. Since the comparator threshold voltage depends linearly on the control code, as shown in Figure 5, the control code can be obtained for a good decision (DTFk) from (15):

$$DTFk = DTCk - DTOk/8 + DTOk \quad (k=1,2,\ldots,7).$$

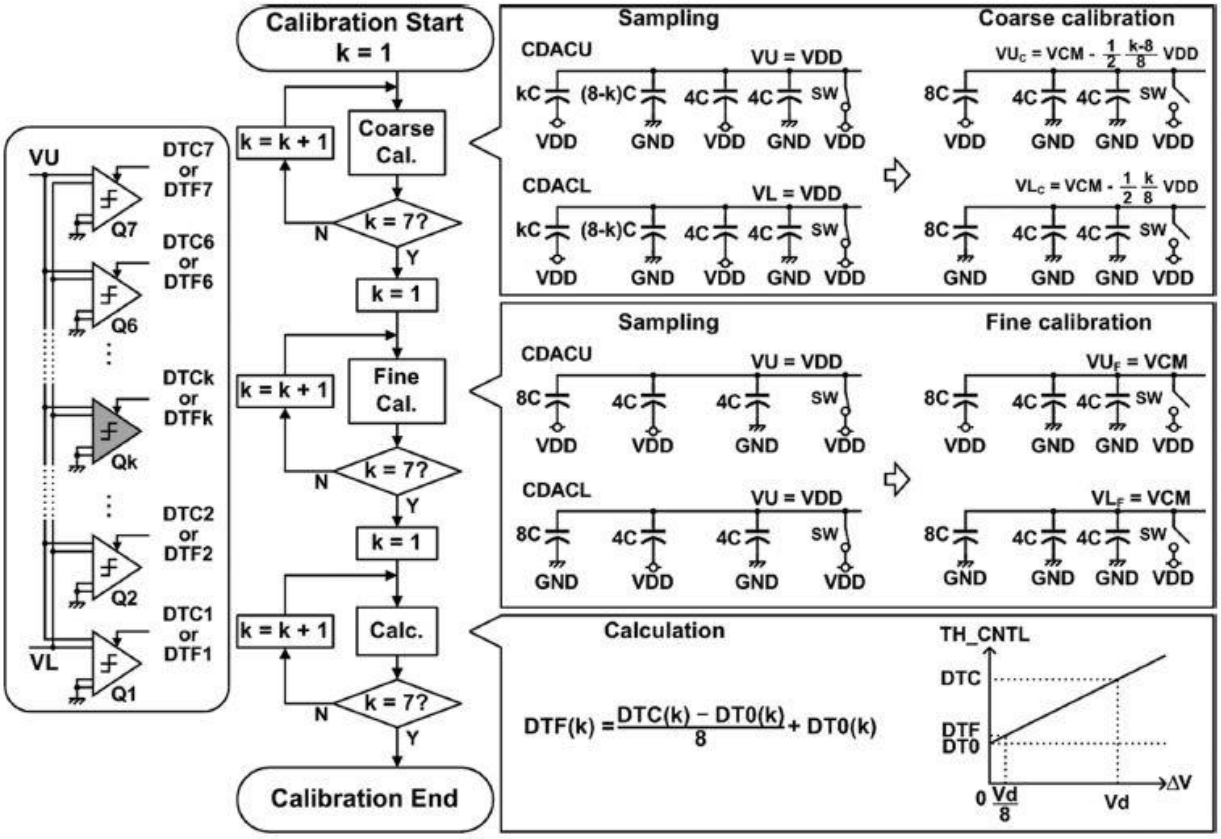

Fig. 6. Flow chart for the foreground calibration.

All calibration circuits run on the chip and do not require manual off-chip adjustment. Because the calibration is done in the foreground, it cannot compensate for the resulting changes and temperature changes that occur afterward. Circuit simulations showed that a 15% decrease from the maximum value (1.3 volts) causes the SNDR to break down by 2 dB, and a change in temperature from -40 ° C to 125 ° C causes the SNDR to change by less than 1 dB. Re-calibration is required if better accuracy is required.

RESULTS

The measured DNL and INL (with and without calibration) are shown in Fig. 7. Before calibration, the DNL and INL each reach 3 LSB. After calibration, they are reduced to 0.8 LSB. The measured spectrum after calibration is shown in Fig. 8. Here, the sampling frequency is 1 GS/s, and the input signal frequency is 501 MHz. The SNDR is 32.8 dB, resulting in 5.16 ENOB at the Nyquist frequency. Here, the output data is decimated by a factor of eight due to limitations in the measurement instruments. SNDR and SFDR are plotted against input frequency in Fig. 9. SNDR stays above 32.8 dB up to the Nyquist frequency. Table I summarizes the performance of the proposed ADC. The power consumption of the whole circuit (including calibration) is 9.9 mW, and FoM is 278 fJ/conv.-step at a 1.1-V supply voltage. The clock drivers account for 40% of the total power, the comparators 22%, the threshold-level controller 32%, and the CDACs 6%.

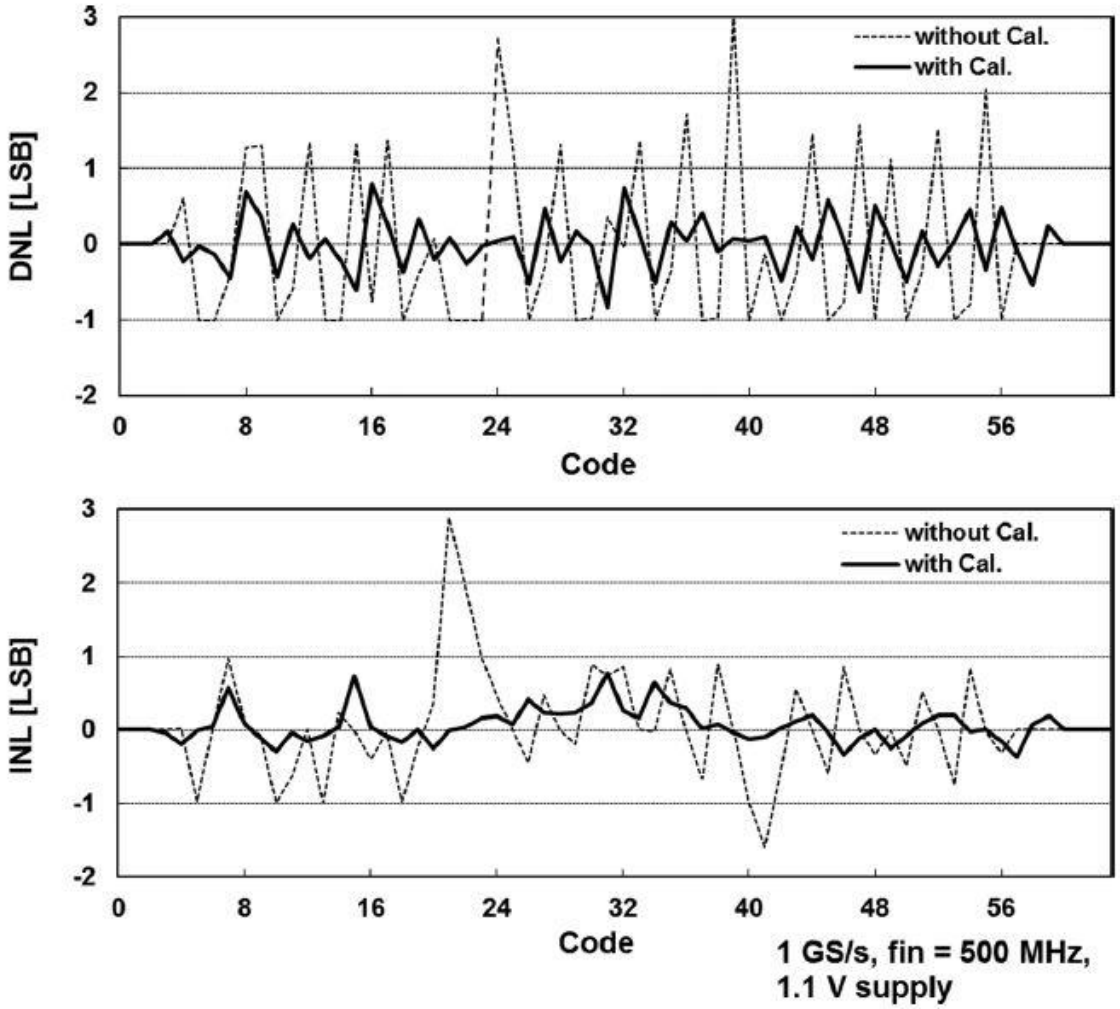

Fig. 7. Measured DNL and INL.

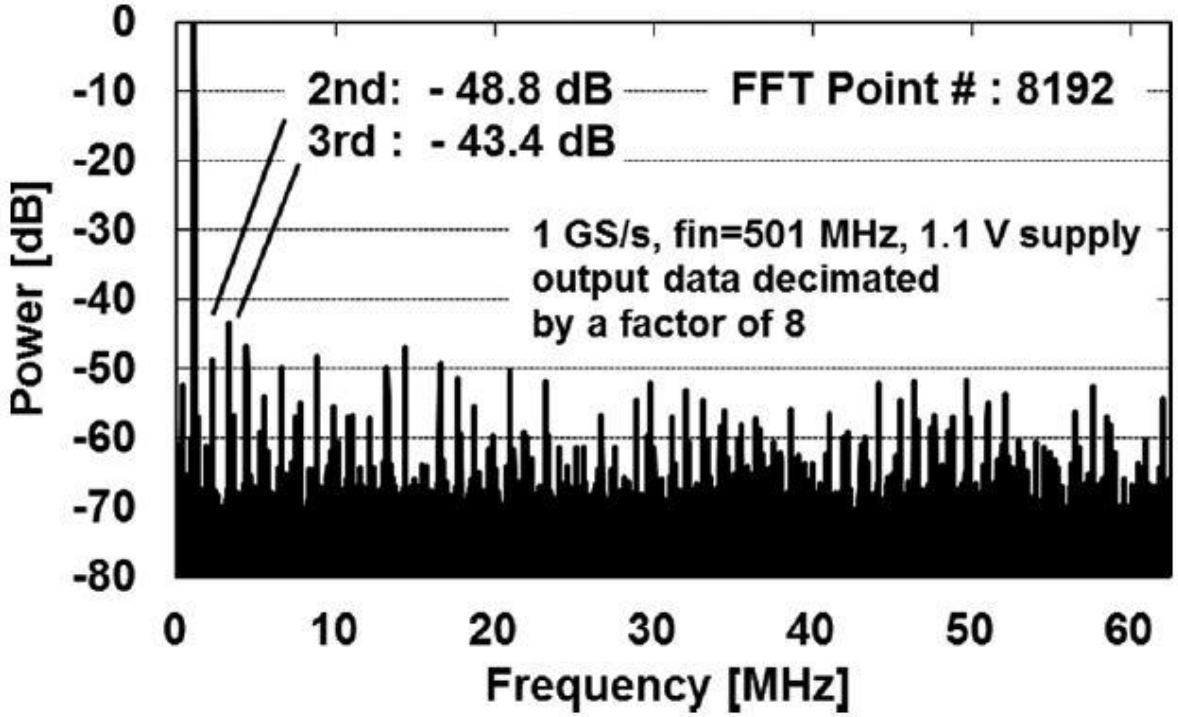

Fig. 8. Measured spectrum.

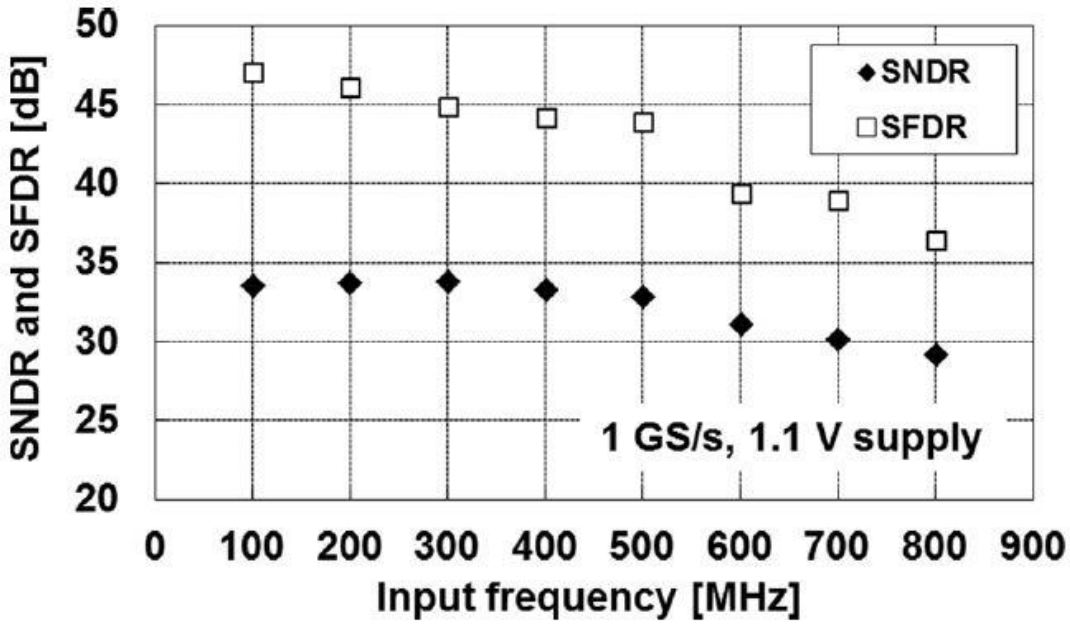

Fig. 9. SNDR and SFDR vs. input frequency.

CONCLUSION

Better substructure architecture is provided to deal with issues arising from reference voltage settling times and switches connected to potential intermediate nodes in subset ADCs. In this ADC architecture, the reference voltage generator and its associated switches are removed using the CDAC, and the comparator threshold level is digitally controlled using active interpolation. In addition, to reduce ADC levels and sampling error, the same set of comparators (no additional comparators) is used for large and good decisions. To realize this architecture, different threshold control codes for large and good decisions are provided to each comparator. A digital control circuit generates a threshold control code for a large decision by generating a nominal voltage with CDAC. Good decision code is obtained by coarse code using digital computing instead of high-resolution DAC, and all calibrations are performed on the chip.

Acknowledgments

None

Conflict of interest

None

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None

Ethics statement

None

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